MEMS fabrication techniques for miniaturization of cylindrical ion trap arrays

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Outline

Part I

- Brief overview of ion traps
- Simulations of ion traps
- Some validating experiments

Part II

- Micro CIT-MS and simulations

Part III

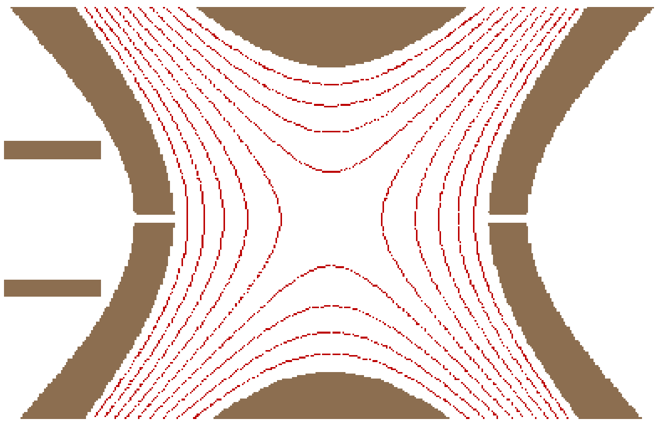
- MEMS fabrication of micro ion traps.
- Results

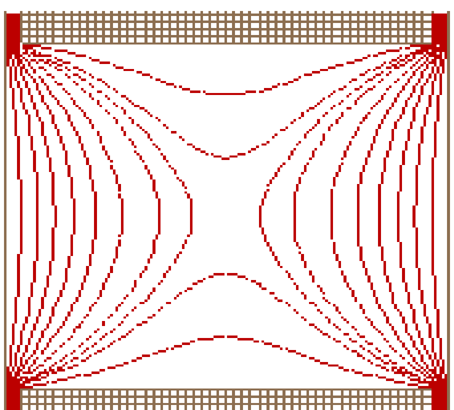
PART I

- Brief overview of ion traps
- Simulations of ion traps
- Some validating experiments

Brief overview of ion traps.

-RF electric potential of hyperbolic and cylindrical ion trap.





Analytical solution of electric potential (no endplate spacing end endplate apertures)

Multipole components are:

$$A_2^{\mathrm{R}} = 1$$

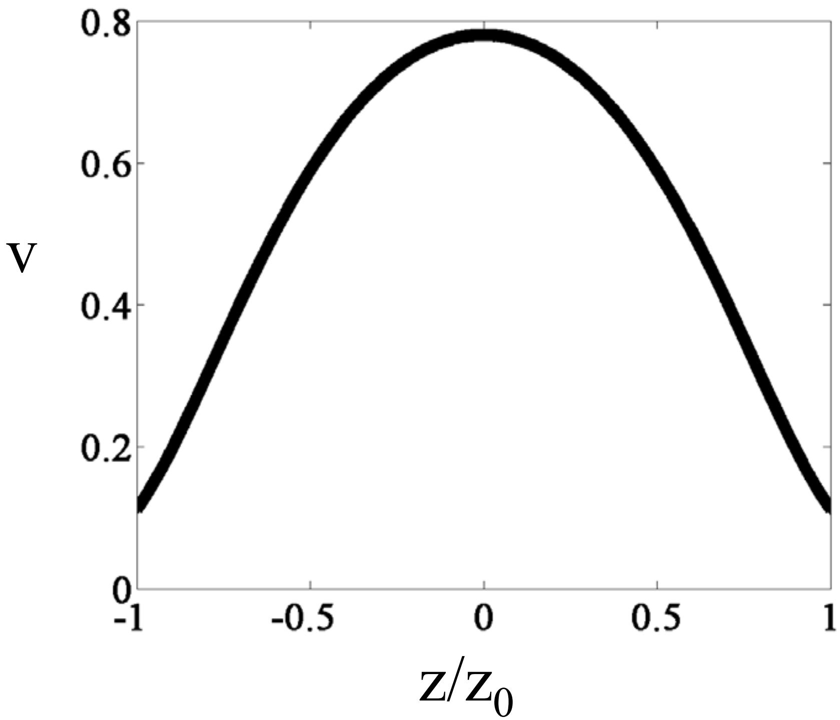
[1]

$$A_{2n}^{\mathrm{R}} = -\frac{2}{(2n)!} \cdot \sum_{i=1}^{\infty} \frac{x_i^{2n-1}}{\cosh\left(\frac{z_0}{r_0} x_i\right) \mathrm{J}_1(x_i)} + \delta_{n,0}$$

[1] O. Kornienko, P. T. A. Reilley, W. B. Whitten, and J. M. Ramsey, "Micro Ion Trap Mass Spectrometry" Rapid Commun. Mass. Spectrom., vol. 13, pp 50-53, Nov. 1999.

Simulations for ion traps.

Simulations in SIMION (D.A. Dahl) or fly an electron through CIT in SIMION to record potential on z-axis.



Least Square Fit (LSQF) gives multipoles.

Simulations in ITSIM (Purdue, R.G. Cooks).

Optimization Predictions.

Proof of concept. Step 1.

Analytical multipoles for CIT $z_0/r_0=0.9$.[1,2]
Multipoles in right column are obtained from LSQF from SIMION potential.

Multipole number	Analytical multipole	LSQF multipole
A2	-0.848387	-0.848364
A4	-0.072415	-0.072439
A6	0.182100	0.182070
A8	-0.003054	-0.003010

Prior work of R.G. Cooks for CIT-0 with endcap holes and endcap spacing.[3]

Multipole number	G. Wu et al.	LSQF multipole
A2	0.736	-0.736
A4	0.055	-0.054
A6	-0.131	0.132

Ring electrode was chosen +1 volt endplates were grounded, thus - sign inverted.

1 O. Kornienko, P. T. A. Reilley, W. B. Whitten, and J. M. Ramsey, "Micro Ion Trap Mass Spectrometry" Rapid Commun. Mass. Spectrom., vol. 13, pp 50-53, Nov. 1999.

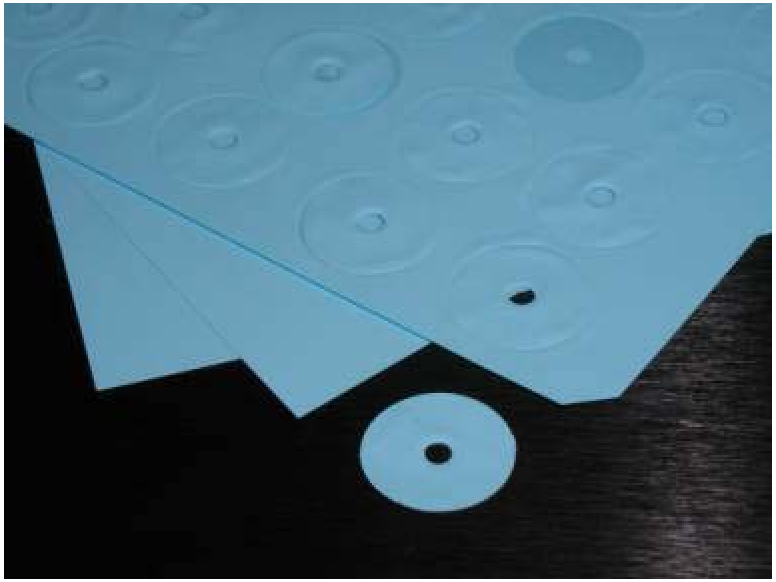
2 W. R. Plass, " Ph.D. Thesis, "The Dependence of RF ion Trap Mass Spectrometer Performance on Electrode Geometry and Collisional Processes" Justus-Liebig-Universität Giessen, Germany, 2001.

3 G. Wu, R. G. Cooks, and Z. Ouyang, "Geometry optimization for the cylindrical ion trap: field calculations, simulations and experiments" Int. J. Mass Spectrom., vol. 241, pp 119-132 (2005).

Some validating experiments

Low Temperature Co-fired Ceramics (LTCC)

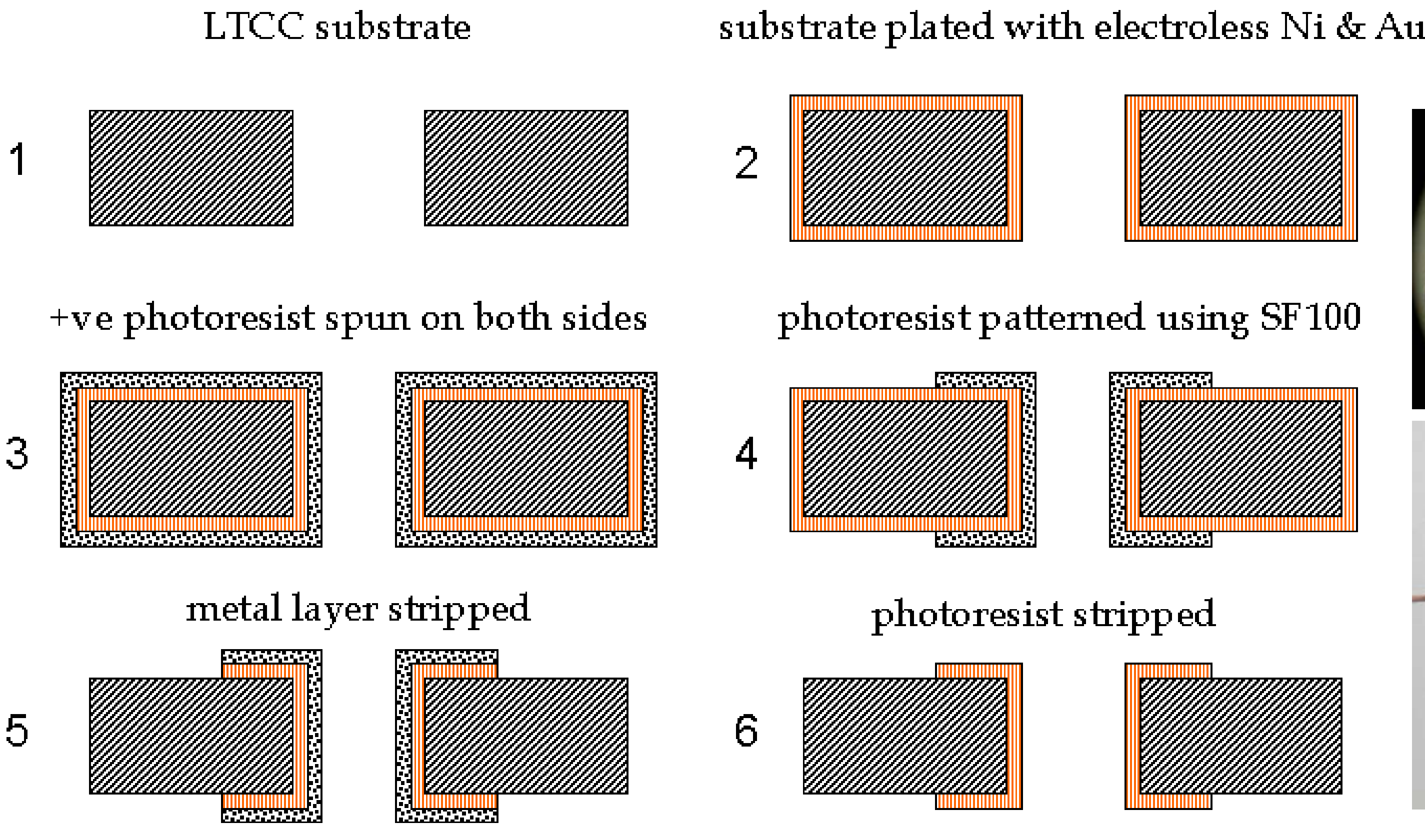
- Soft pliable tapes that turn into hard ceramics when fired at 850°C
- Easily shaped into 3-D structures
- Chemically inert
- Easily made conductive on surface using electroless plating.

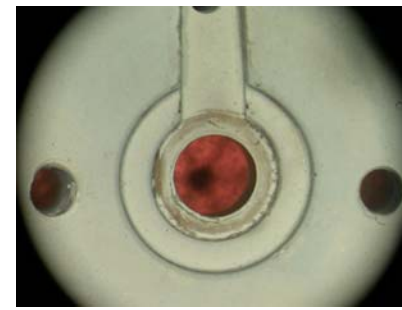


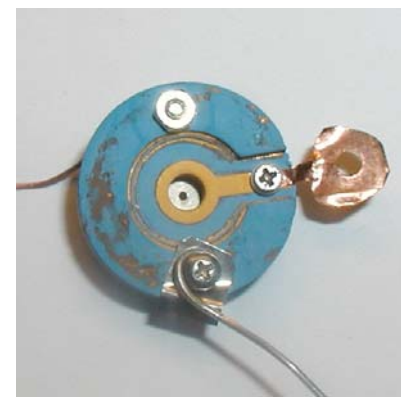
Die used to shape LTCC into a ring electrode.

Step to align endplates.

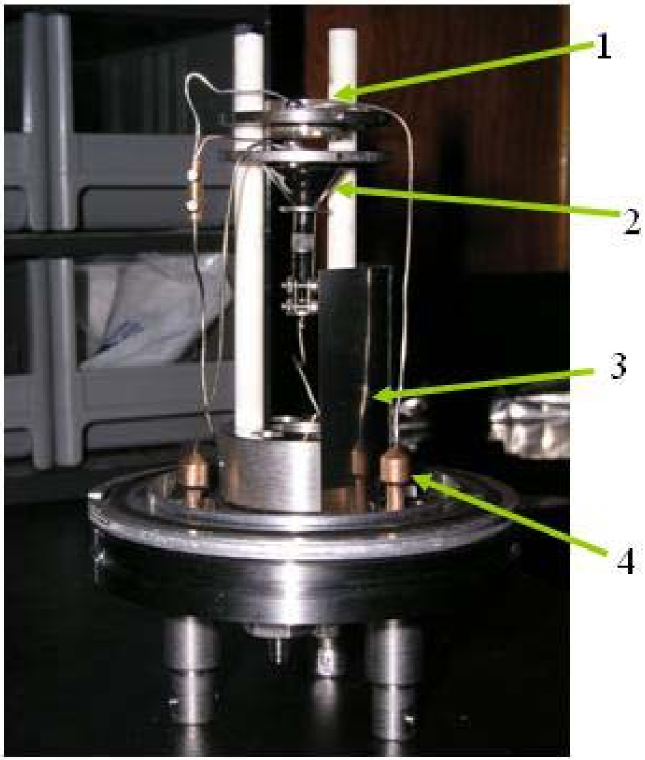
Some validating experiments



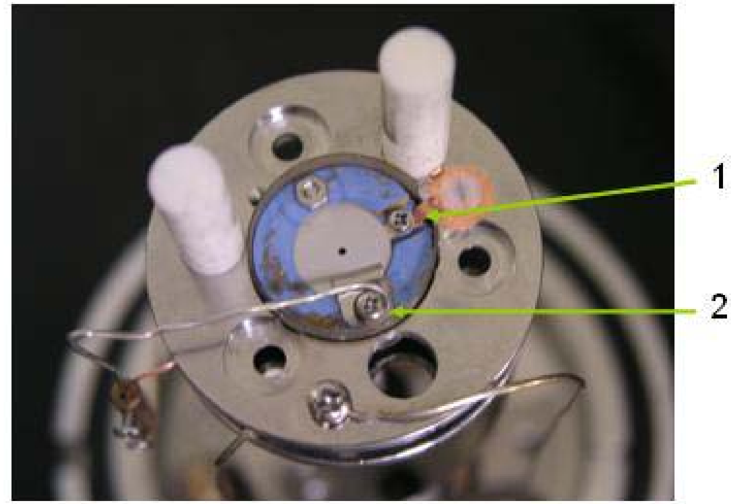




Some validating experiments

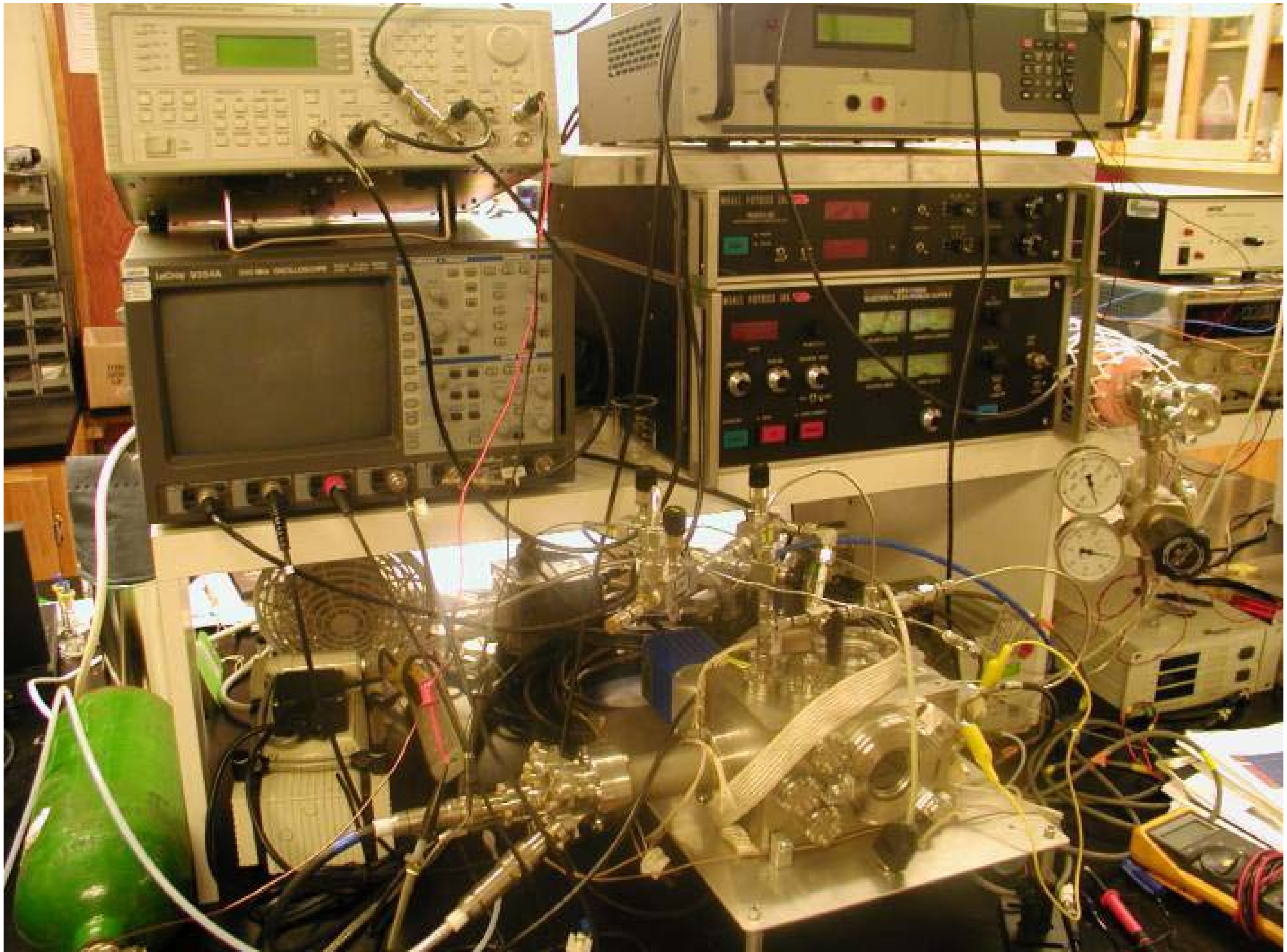


1) LTCC CIT
2) Detector (Detech)
3) RF shielding
4) RF electrical feed through connector



1) Cylinder electrode connection
2) Endplate connector grounded

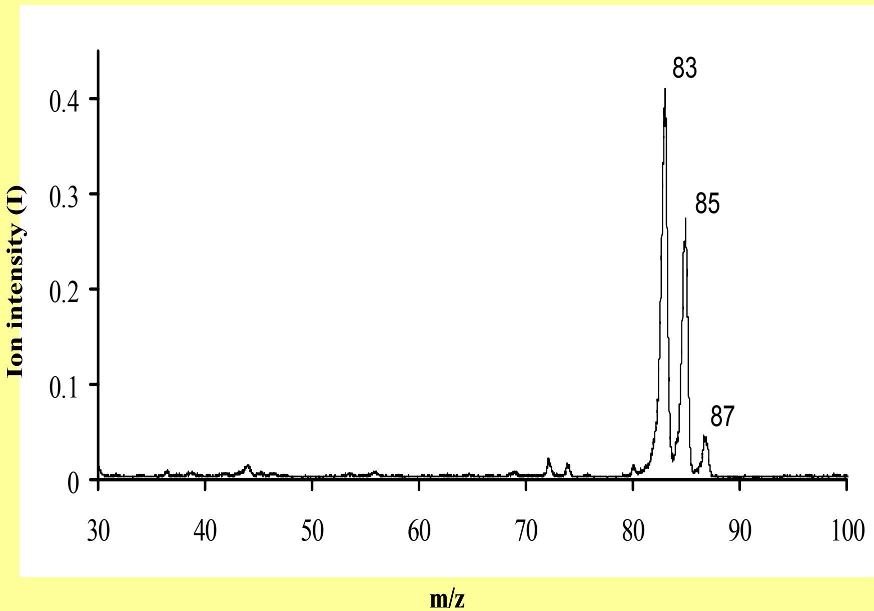
Some validating experiments



Laboratory setup

Proof of concept. Step 2.

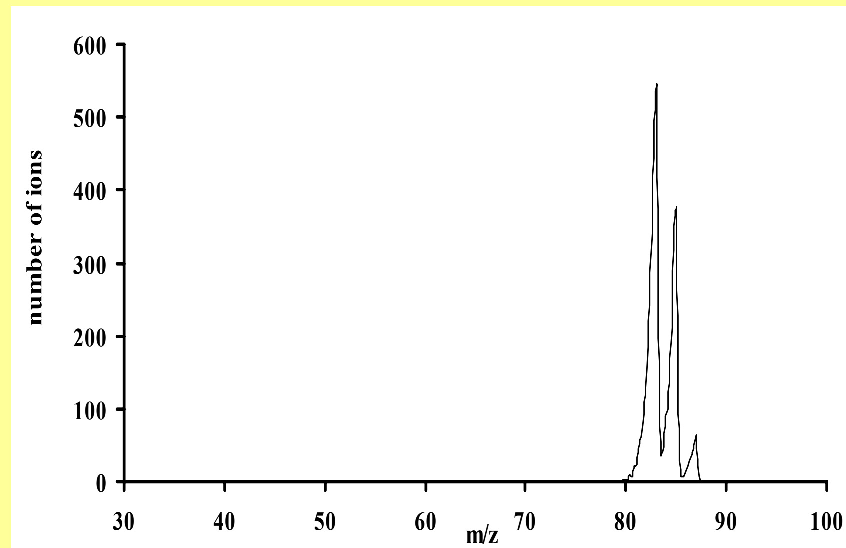
LTCC CIT experiments.
Chloroform as analyte.



Multipole determination of LTCC trap.

A2	-0.7349
A4	-0.1739
A6	0.2060

→ Sign inverted and used in ITSIM

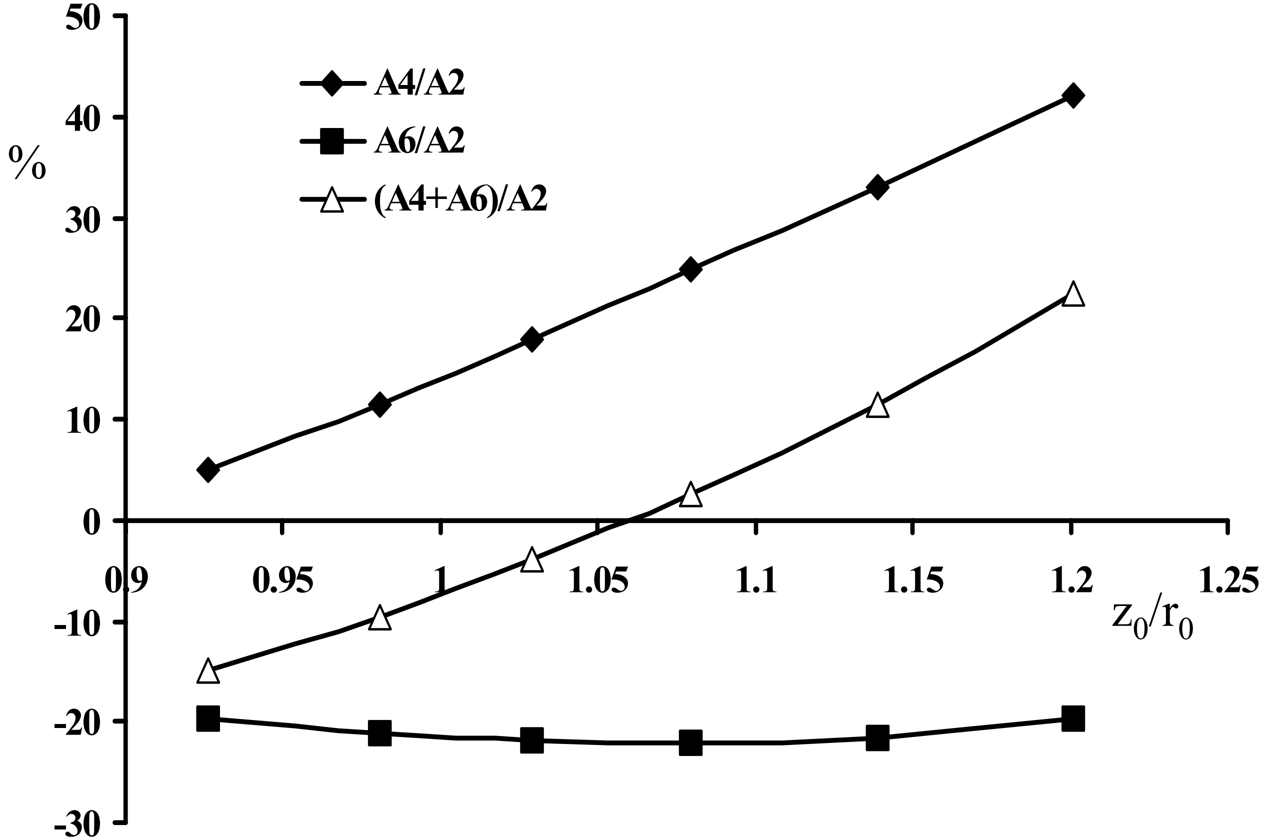


Simulations in ITSIM on LTCC CIT geometry.

PART II

- Micro CIT mass spectrometers and simulations

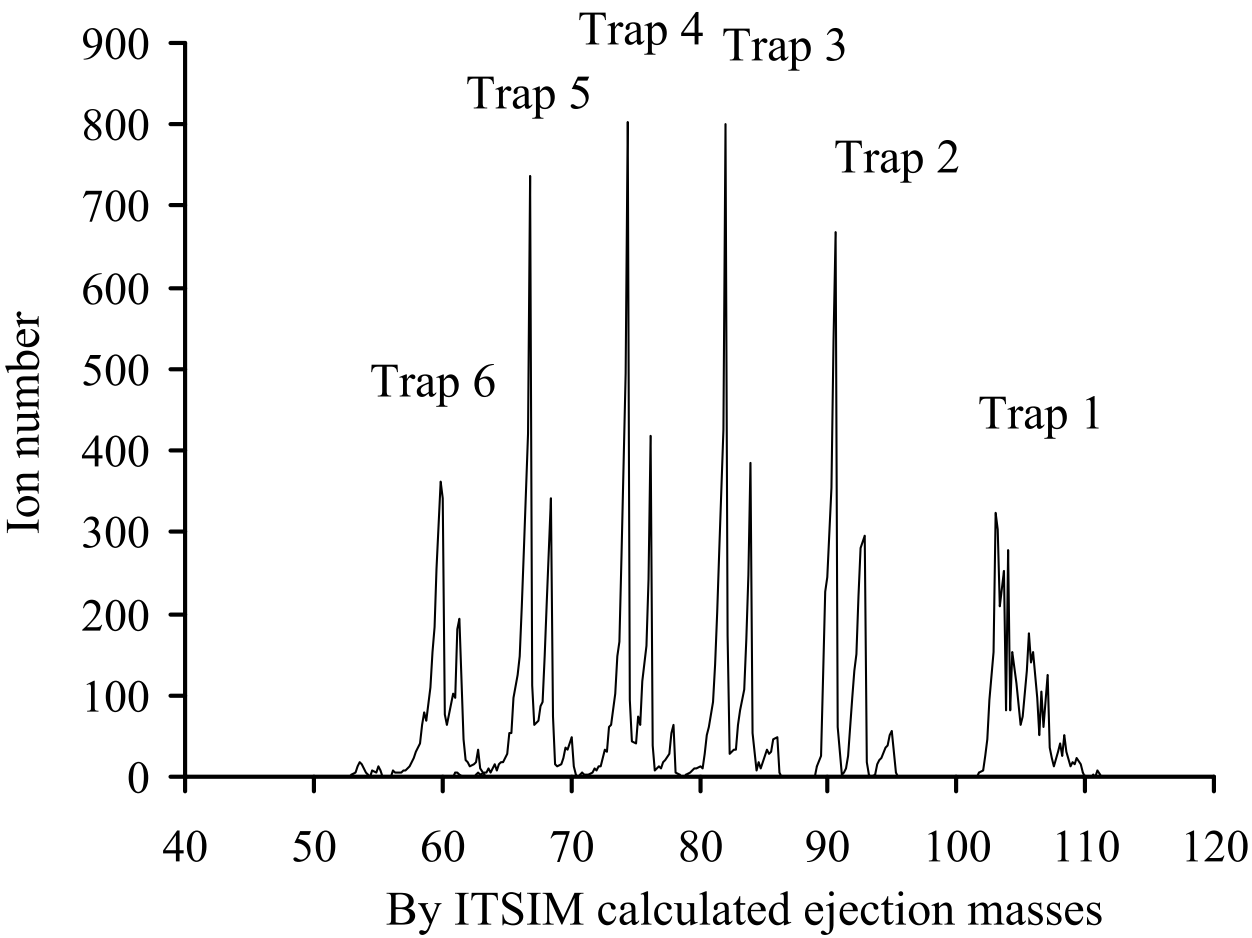
Determination of the multipoles of micro CIT electric potential.



$z_0 = 350\ \mu m$

Trap #	z_0/r_0	r_0 μm
1	0.92	381
2	0.97	360
3	1.02	343
4	1.07	327
5	1.13	310
6	1.19	294

Simulated spectra of $CHCl_2^+$ for micro CIT-MS.



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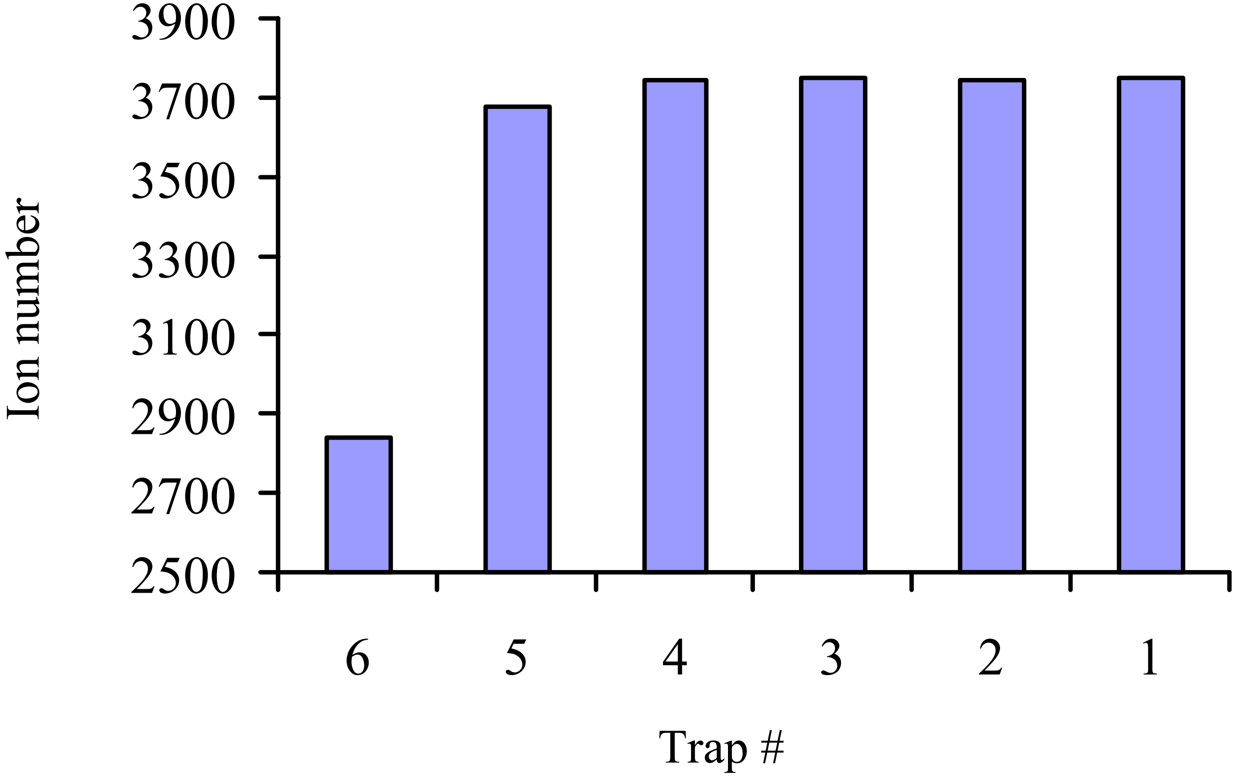
Optimum geometry for simulated CIT trap somewhere between trap 2 and 6.
(no axial modulation used, Investigated with low kinetic energy to visualize details.)

Ion loss on electrodes when stretching geometry.



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When CIT geometry over stretched ion loss on electrodes occurs.

PART III

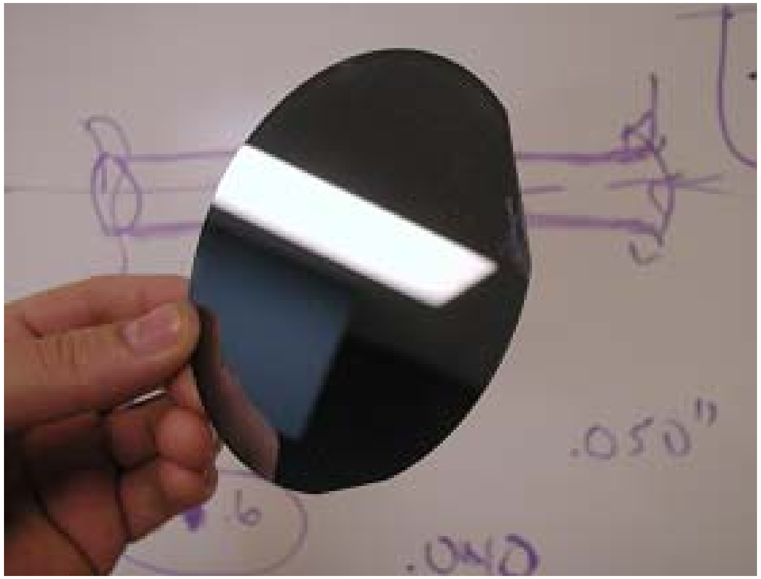
- MEMS fabrication of micro ion traps

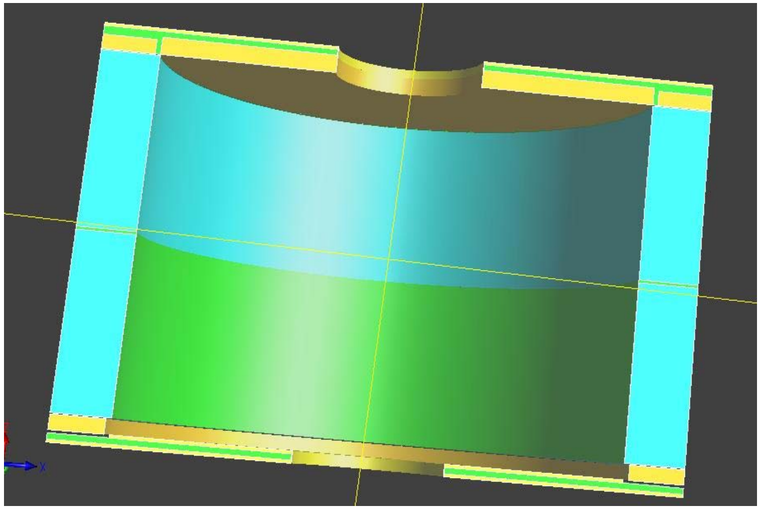
MEMS facilities

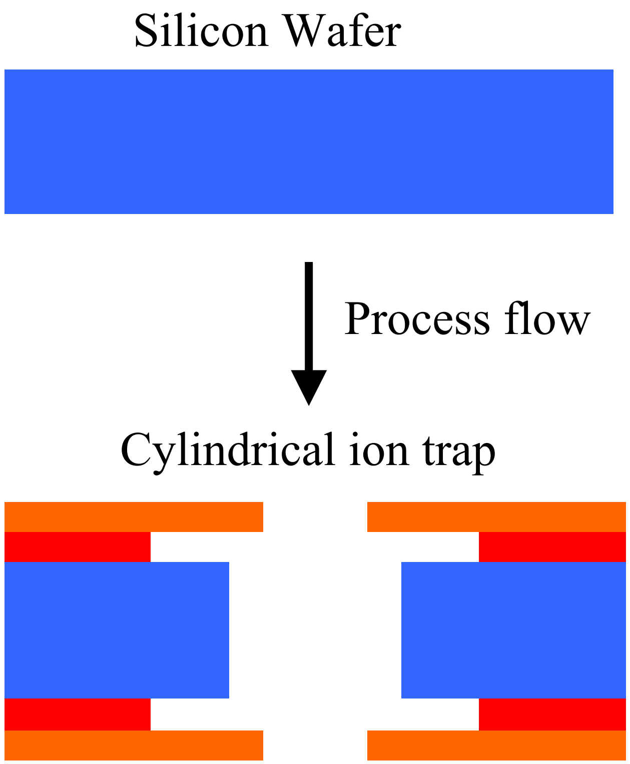
Analytical bay contains the JEOL SEM, the Hitachi high resolution SEM and the FEI dual beam FIB.

The dry processing bay shows the PECVD, RIE, DRIE, ebeam evaporator, 4 tube LPCVD and 2 sputtering systems.

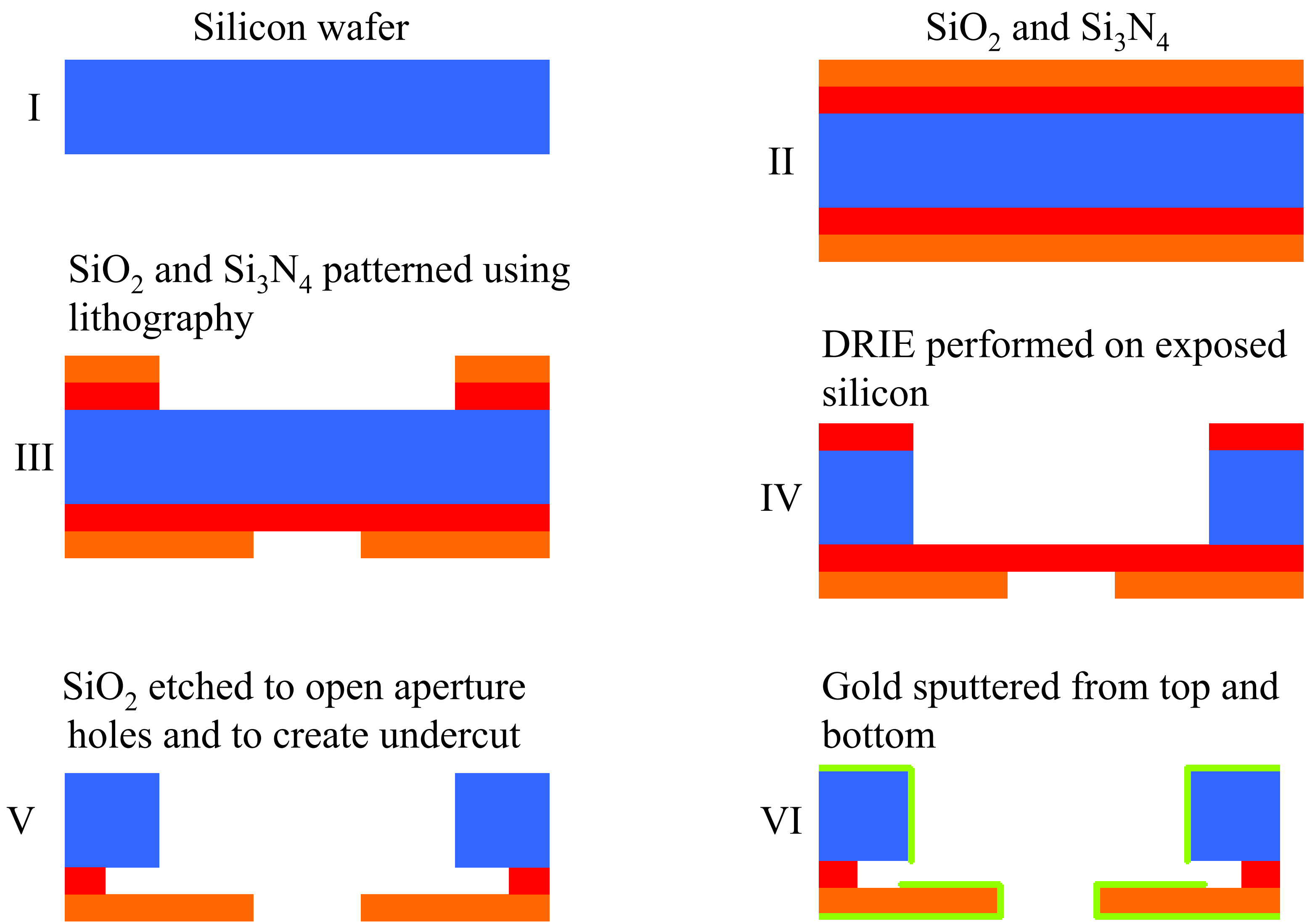
MEMS fabrication process flow



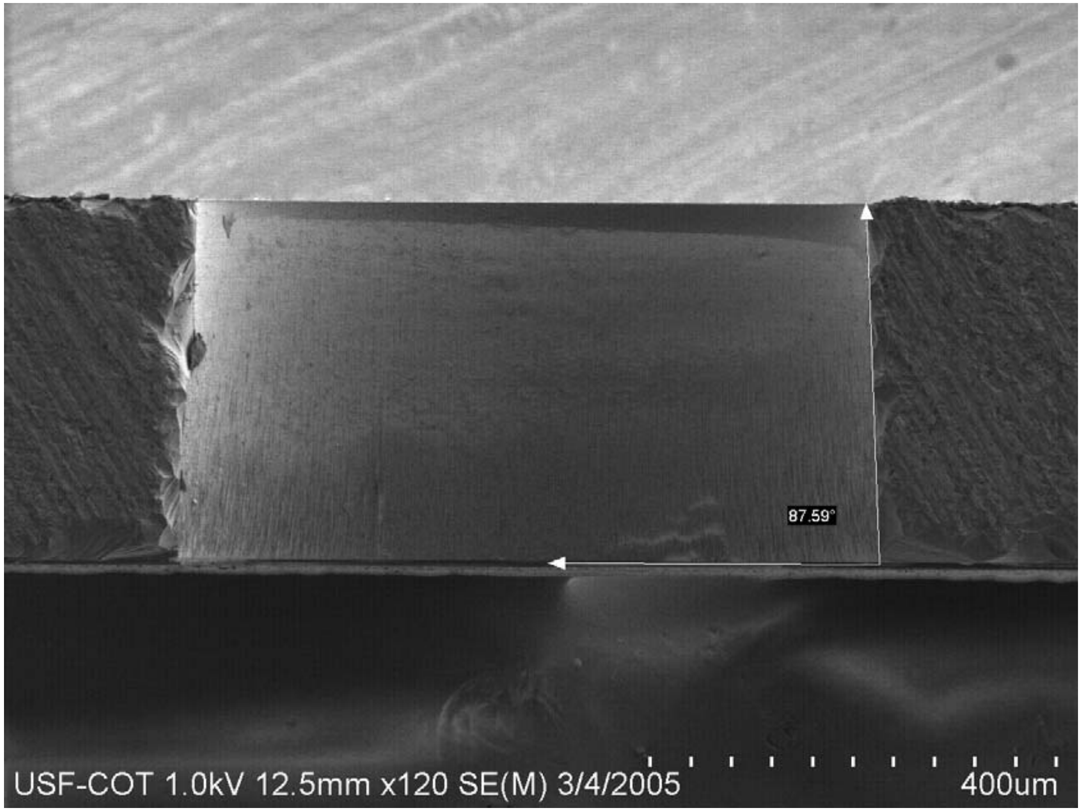




MEMS fabrication process flow

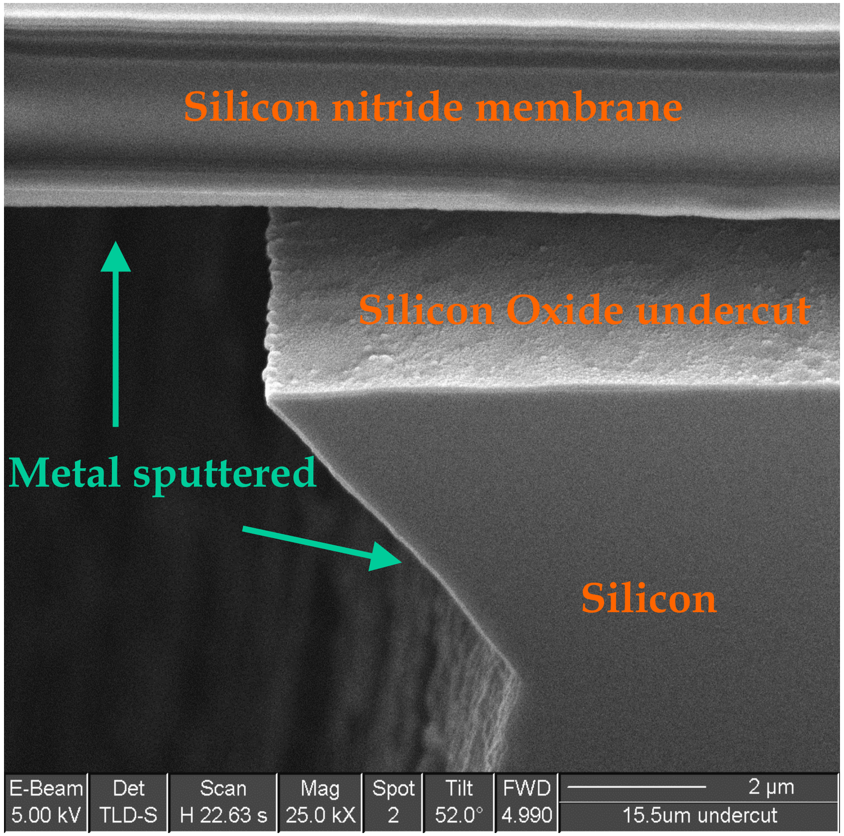


MEMS fabrication process flow

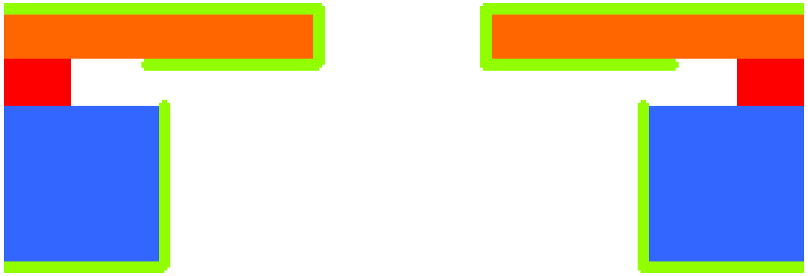


DRIE performed on exposed silicon

MEMS fabrication process flow



Gold sputtered from top and bottom



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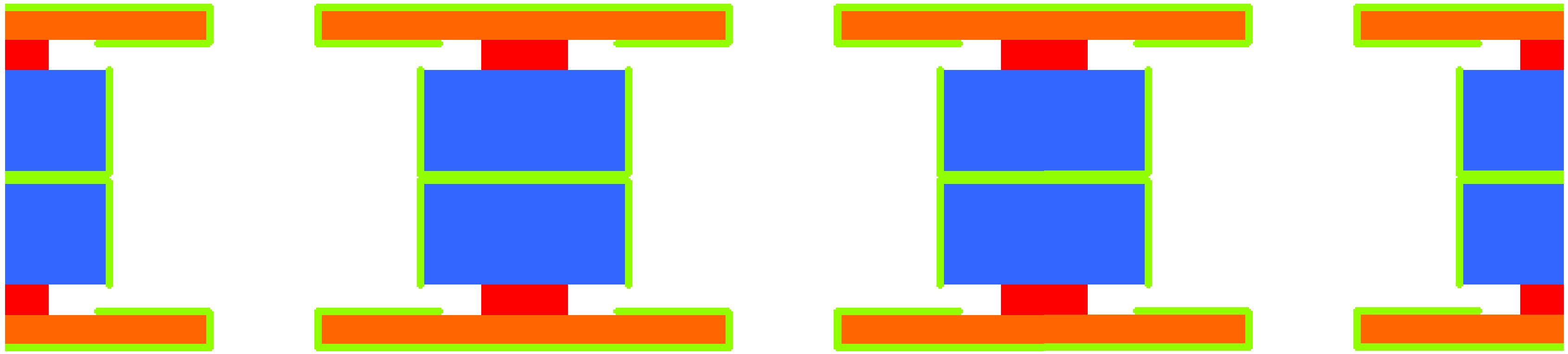


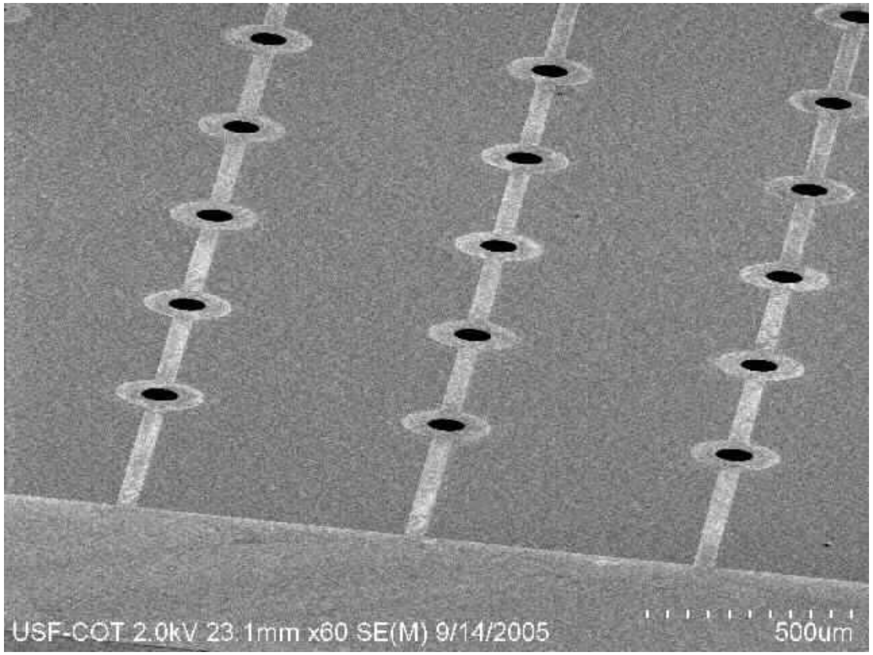
- Diced half structures bonded (Au thermal compression bonding, or conducting epoxy) to obtain CIT arrays.

- Z_0 (wafer thickness) can be changed to obtain many different sizes of CITs.

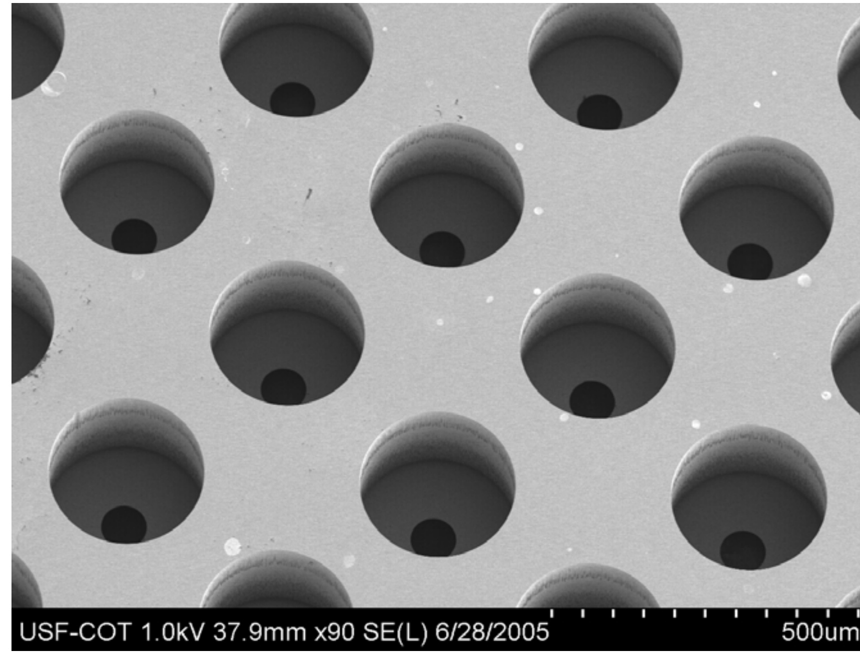
MEMS operators

CIT arrays

Results

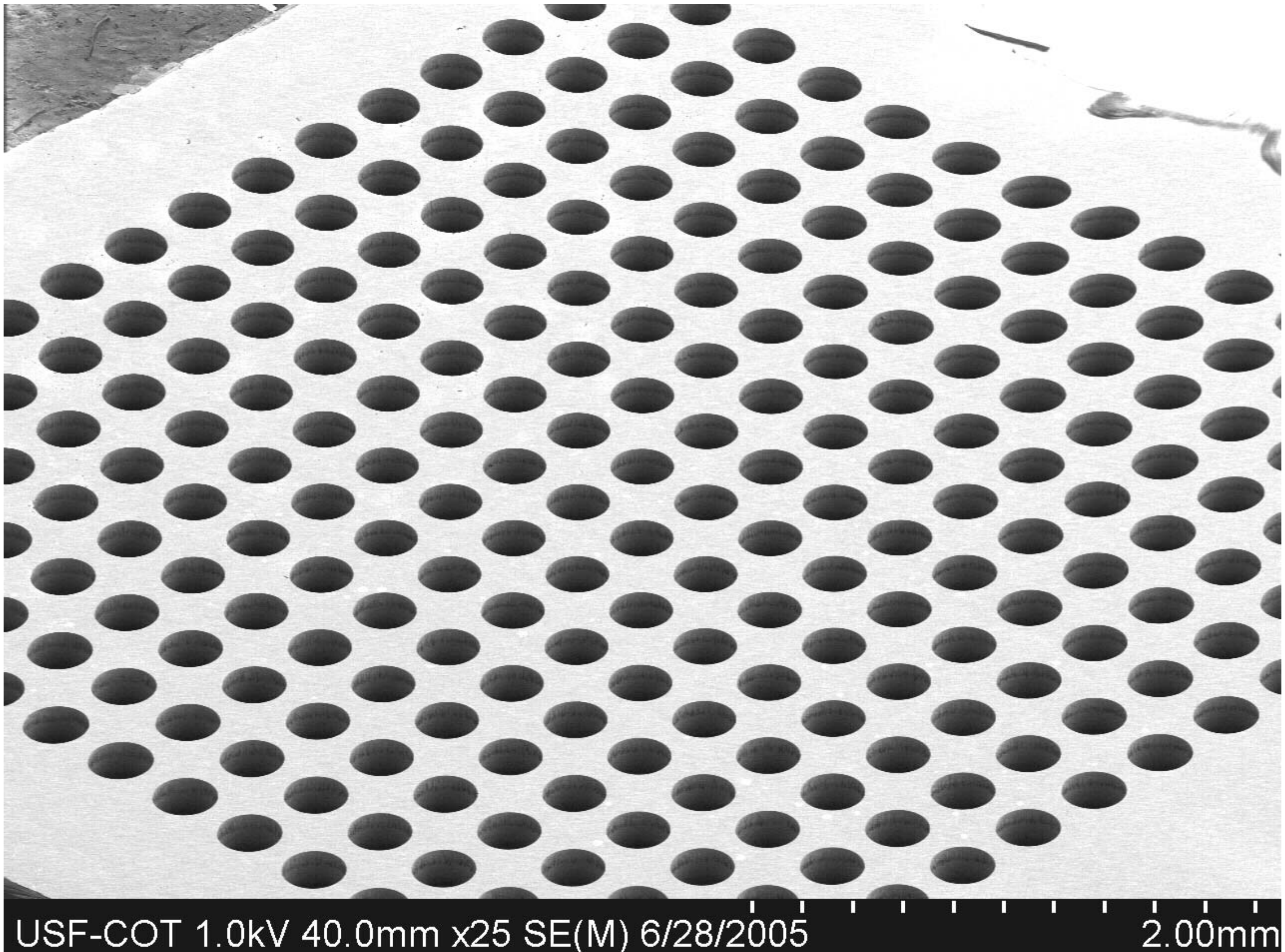


Capacitance reduction is achieved by reducing the conductive area on outer surfaces surrounding the apertures.

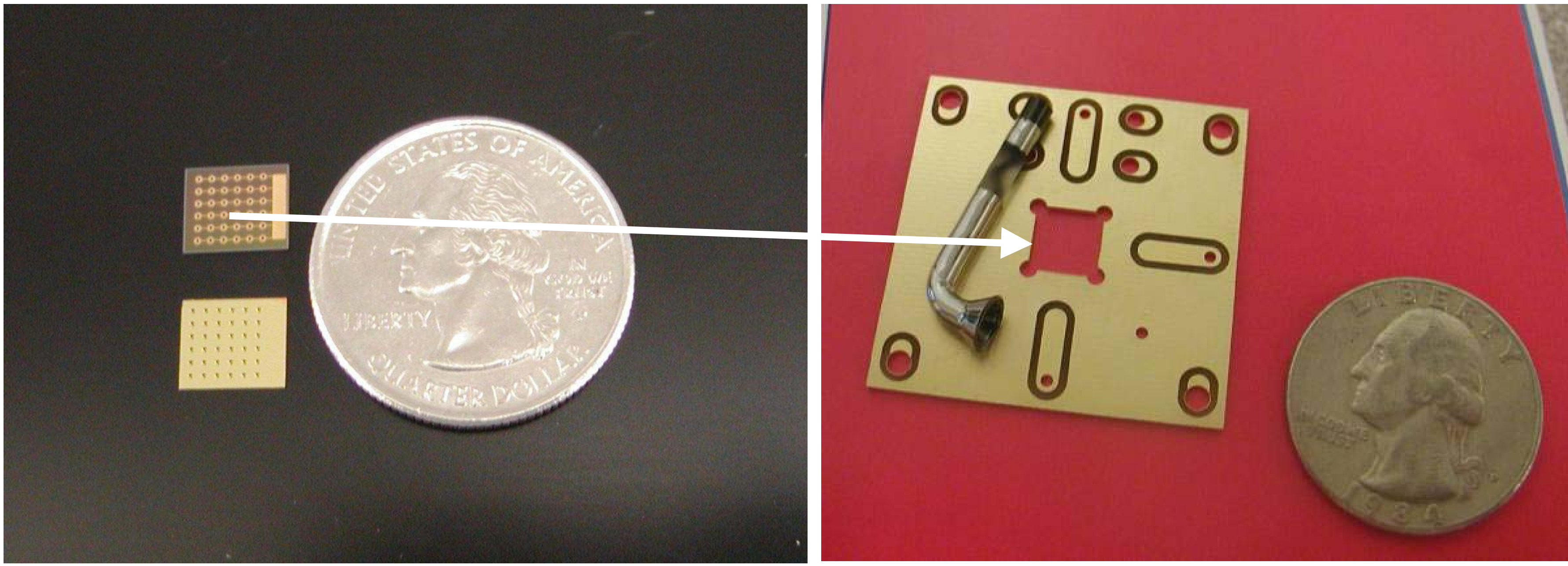


CIT half structure with endplate aperture shown in the bottom of the cylindrical electrode.

Results



Packaging method



Discussions

Simulations

- At least 1000 gnu (SIMION) on z-axis necessary for correct multipole determination.
- Are simulation results for smaller trap sizes valid ?
- When CIT geometry is over stretched ion loss on electrodes occurs.

MEMS fabrication

- Process flow to be optimized further.
- Optimization of micro CIT’s should be fast due to large range of trap sizes available per processed wafer.

Acknowledgement

R.G. Cooks et. al for providing ITSIM.

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